Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A semiconductor memory comprising:

an error detector circuit which, based on first data read out from a memory cell and second data provided to an external input terminal, determines whether the memory cell is good or faulty; and

a self fuse program circuit which, when the memory cell is faulty, programs address data for the memory cell as save address data in an electrical fuse;

wherein the error detector circuit has an output circuit, and the output circuit is deactivated when the first data is read out from the memory cell.

2. (Canceled)

3. (Currently amended) ~~The~~ A semiconductor memory ~~according to claim 2,~~ comprising:

an error detector circuit which, based on first data read out from a memory cell and second data provided to an external input terminal, determines whether the memory cell is good or faulty; and

a self fuse program circuit which, when the memory cell is faulty, programs address data for the memory cell as save address data in an electrical fuse,

wherein the error detector circuit has a comparator circuit, and the comparator circuit has a function for comparing the first data with the second data, and in the case where values of both data do not coincide with each other, outputting a sense signal, and

wherein the error detector circuit has an input circuit, and the input circuit has a function for inputting third data to be programmed for the memory cell and inputting the second data.

4. (Original) The semiconductor memory according to claim 3, wherein the second data and the third data has an identical value.

5. (Original) The semiconductor memory according to claim 4, wherein the error detector circuit has a pseudo read control circuit, and the pseudo read control circuit has a function for transferring the second data to the comparator circuit and transferring the third data to the memory cell.

6. (Original) The semiconductor memory according to claim 5, wherein, after the third data has been programmed for the memory cell, the first data is read out from the memory cell.

7. (Canceled)

8. (Currently amended) The semiconductor memory according to claim ~~7~~ 1, wherein the error detector circuit has a pseudo read control circuit, and the pseudo read control circuit has a function for transferring the first data to ~~the~~ a comparator circuit.

9. (Currently amended) ~~The~~ A semiconductor memory ~~according to claim 2,~~ comprising:

an error detector circuit which, based on first data read out from a memory cell and second data provided to an external input terminal, determines whether the memory cell is good or faulty; and

a self fuse program circuit which, when the memory cell is faulty, programs address data for the memory cell as save address data in an electrical fuse,

wherein the error detector circuit has a comparator circuit, and the comparator circuit has a function for comparing the first data with the second data, and in the case where values of both data do not coincide with each other, outputting a sense signal, and

wherein the self fuse program circuit has a latch circuit, and the latch circuit has a function for latching the address data upon receipt of the sense signal.

10. (Original) The semiconductor memory according to claim 9, wherein the latch circuit has a function for latching master data for validating the address data as the save address data upon receipt of the sense signal.

11. (Original) The semiconductor memory according to claim 10, wherein the latch circuit has a function for latching a bank selection signal for selecting a bank including the memory cell upon receipt of the sense signal.

12. (Original) The semiconductor memory according to claim 11, wherein the latch circuit determines whether or not to output the master data and the save address data based on the bank selection signal.

13. (Original) The semiconductor memory according to claim 9, wherein the self fuse program circuit has a fuse program circuit, and the fuse program circuit has a function for programming the save address data for the electrical fuse.

14. (Original) The semiconductor memory according to claim 13, wherein the self fuse program circuit has a counter and a switch circuit, and the counter and the switch circuit have a function for transferring the save address data to the fuse program circuit on one bit by one bit basis.

15. (Original) The semiconductor memory according to claim 14, wherein the save address data is configured of a plurality of bits, and a programming operation for the electrical fuse is carried out for all bits irrespective of a value of each bit of the save address data.

16. (Original) The semiconductor memory according to claim 15, further comprising a monitor circuit which monitors data programmed for the electrical fuse.

17. (Original) The semiconductor memory according to claim 16, wherein, when a verifying operation for. monitoring data programmed for the electrical fuse is carried out, all bits of the save address data are set to an identical value.

18. (Original) The semiconductor memory according to claim 17, wherein the counter is initialized before carrying out a verifying operation.

19. (Original) The semiconductor memory according to claim 14, wherein the self fuse program circuit has a bank selector circuit, and the bank selector circuit has a function for, when the fuse program circuit corresponds to a selected bank, transferring the save address data to the switch circuit.